WHAT IS CLAIMED IS:

1. A clock control circuit comprising:

means for generating and outputting an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock period of said reference clock, said reference clock being an input clock or a clock derived from the input clock.

2. A clock control circuit comprising:

control means for producing a control signal for adding or subtracting to or from a phase relative to a reference clock, by a predetermined unit value of a phase differential, on each clock period of said reference clock, said reference clock being an input clock or a clock generated from the input clock; and

phase adjustment means fed with the input clock for generating an output clock having a phase relative to said reference clock, said phase being added or subtracted by the predetermined unit value of the phase differential based on said control signal; whereby said output clock of a frequency is allowed to be in a non-integer relation with respect to a frequency of said reference clock.

3. A clock control circuit comprising:

a control circuit for generation of a control signal for adding or subtracting to or from a phase difference of an output clock relative to an input clock by a unit value of a phase difference; and

a phase adjustment circuit fed with said input clock for generating and outputting an output clock having said phase difference prescribed

by said control signal.

4. A clock control circuit comprising:

a frequency dividing circuit fed with an input signal to frequency divide the input clock to output an frequency divided clock;

a control circuit for generation of a control signal adding or subtracting to or from a phase difference relative to said frequency divided clock by a unit value of a phase difference based on the frequency divided clock output from said frequency dividing circuit; and

a phase adjustment circuit fed with said input clock and generating and outputting an output clock having said phase prescribed by said control signal from said control circuit.

5. A clock control circuit comprising:

a multi-phase clock generating circuit for generating and outputting first to nth clocks having respective difference phases from an input clock received;

a selector fed with said first to nth clocks to select and output one of said first to nth clocks; and

a control circuit fed with an input clock to generate a selection signal for selecting sequentially said first to nth clocks to provide the generated selection signal to said selector.

6. The clock control circuit as defined in claim 4 wherein

said unit value of the phase difference is variably set by a mode signal input from outside.

7. The clock control circuit as defined in claim 5 wherein

an output of the selection signal controlling selection of said

selector is variably set by a mode signal input to said control circuit.

8. A clock control circuit comprising:

a multi-phase multiplication clock generating circuit receiving an input clock to generate first to nth clocks of respective different phases(termed multi-phase multiplication clocks) obtained by frequency multiplying said input clock;

a switch for selecting two clock signals of said first to nth clocks output from said multi-phase multiplication clock generating circuit;

at least one interpolator receiving the two clock signals selected and output by said switch to generate an output signal, a propagation delay of said output signal corresponding to division of timing difference of said two clock signals, with a ratio of a internal division being variably set; and

a control circuit for producing a switching signal for said switch and a control signal for variably setting a ratio of internal division of the timing difference of said interpolator.

9. A clock control circuit comprising:

a multi-phase multiplication clock generating circuit receiving an input clock to generate first to nth clocks of respective different phases(termed multi-phase multiplication clocks) obtained by frequency multiplying the input clock;

a switch for selecting two sets each of two neighboring ones of said first to nth clocks output from said multi-phase multiplication clock generating circuit;

a first interpolator receiving the first set of two clocks output from

said switch to generate a first signal, a propagation delay of said first signal corresponding to division of timing difference of said two clock signals;

a second interpolator receiving the second set of two clocks output from said switch to generate a second signal, a propagation delay of said second signal corresponding to division of timing difference of said two clock signals;

a third interpolator receiving said first and second signals of said first and second interpolators to generate a third signal, a propagation delay of said third signal corresponding to division of timing difference of said first and second signals;

a ratio of the internal division of the timing difference of at least one of said first to third interpolators being variably set; and

a control circuit for outputting a switching signal for said switch and a control signal for variably setting the ratio of the internal division of the timing difference of said interpolators.

10. A clock control circuit comprising:

a frequency divider receiving an input clock to generate two sets of clocks of respective different phases obtained on frequency division of said input clock;

a first interpolator receiving the first set of two clocks output from said frequency divider to generate a first signal, a propagation delay of said first signal corresponding to division of timing difference of said two clock signals;

a second interpolator receiving the second set of two clocks output

from said frequency divider to generate a second signal , a propagation delay of said second signal corresponding to division of timing difference of said two clock signals;

a third interpolator receiving outputs of said first and second interpolators to generate a third signal, a propagation delay of third signal corresponding to division of timing difference of said two outputs;

a ratio of internal division of the timing difference of at least one of said first to third interpolators being variably set; and

a control circuit for outputting a switching signal for said switch and a control signal for variably setting the ratio of internal division of the timing difference of said interpolators.

11. A clock control circuit comprising:

a multi-phase multiplication clock generating circuit receiving an input clock to generate a plurality of clocks of respective different phases (termed multi-phase multiplication clocks) obtained on multiplying the input clock;

a plurality of interpolators receiving respectively two clocks of neighboring phases of said plural clock outputs from said multi-phase multiplication clock generating circuit to output signals corresponding to division with respective different values of the ratio of internal division of the timing difference of said two clocks; and

a synthesis unit fed with outputs of said plural interpolators to multiplex said outputs from said plurality of interpolators to output a s resulting sole output signal.

12. The clock control circuit as defined in claim 11 wherein

said multi-phase multiplication clock generating circuit generates N phase clocks, where N is a preset positive integer, M of said interpolators are provided, where M is a positive integer, such that M $\leqq$ N, an ith one of said interpolators is fed with ith and (i+1)st clocks, where i is an integer from 1 to M, with the (n+1)st clock being a first clock;

a value of a ratio of the internal division dividing the timing difference of two input signals in each of said interpolator being so set that a ratio value of the (i+1)st interpolator is larger or smaller than that of the ith interpolator by a preset unit step;

M-phase clocks being output from said M interpolators; and wherein an output clock of a multiplied by M frequency is output from said synthesis unit.

13. The clock control circuit as defined in claim 5 wherein

said multi-phase clock generating circuit comprises a multi-phase multiplication clock circuit for frequency dividing said input clock to generate multi-phase clocks to generate a signal by frequency multiplying said multi-phase clocks.

14. A clock control circuit as defined in claim 8 wherein

said multi-phase multiplication clock generating circuit comprises a frequency dividing circuit for frequency dividing input clock to generate and output a plurality of clocks of different phases (multi-phase clocks);

a period detection circuit for detecting the period of said input clock; and

a multi-phase clock multiplication circuit fed with the multi-phase

clocks form a frequency dividing circuit to generate multi-phase clocks corresponding to multiplication of said clocks;

said multi-phase clock multiplication circuit comprising:

a plurality of timing difference division circuits for outputting a signal corresponding to division of timing difference of two inputs; and

a plurality of multiplexing circuits multiplexing two outputs of said timing difference division circuits to output the resulting multiplexed signals;

said timing difference division circuits comprising a timing difference division circuit fed with clocks of the same phase and a timing difference division circuit fed with two clocks of neighboring phases.

15. The clock control circuit as defined in claim 14 wherein

said multi-phase clock multiplication circuit is fed with n-phase clocks(first to nth clocks);

there being provided 2n timing difference division circuits for outputting signals corresponding to division of the timing difference of two inputs;

a (2I - 1)st timing difference division circuit, where $1 \leqq I \leqq n$, is fed with the same Ith clocks as said two inputs;

a 2Ith timing difference division circuit, where $1 \leqq I \leqq n$, being fed with the Ith clock and with the (I + 1 mod n)th clock, where mod denotes a remainder operation and I + 1 mod n indicates a remainder of a division of (I + 1) by m;

there being provided 2n pulse width correction circuits fed with an output of a Jth timing difference division circuit, where $1 \leqq J \leqq 2n$,

and with an output of a (J+2 mod n)th timing difference division circuit, where J+2 mod n means the remainder of division of J+2 with n;

there being also provided n multiplexing circuits fed with an output of a Kth pulse width correction circuit, where $1 \leqq K \leqq n$, and with an output of the (K+n)th pulse width correction circuit.

16. The clock control circuit as defined in claim 14 wherein

said timing difference division circuit includes

a NOR circuit receiving first and second input signals; and

an inverter receiving a voltage level of an internal node that is an output of said NOR circuit;

a plurality of series circuits each made up of a switching device and a capacitance device are connected in parallel across said internal node and the ground;

capacitance to be attached to said internal node being determined by a period control signal coupled to a control terminal of said switch.

17. The clock control circuit as defined in claim 14 wherein said timing difference division circuit includes

a logic circuit receiving first and second input signals and outputting a result of a preset logical operation on said first and second input signals;

a first switching device connected across a first power source and an internal node and having an output signal of said logic circuit fed as input to a control terminal thereof;

a buffer circuit an input terminal of which is connected to said internal node and an output logical value of which is changed on inversion

of relative magnitudes of said internal node potential and a threshold value;

a first constant current source connected in series across said internal node and a second switch device and a second switch device controlled on or off by said first input signal; and

a second constant current source connected in series across said internal node and the second power source and a third switching device controlled on or off by said second input signal;

a plurality of series circuits each made up of a fourth switching device and a capacitance device are connected in parallel across said internal node and said second power source;

capacitance to be attached to said internal nod being determined by a period control signal coupled to a control terminal of said fourth switching device.

18. The clock control circuit as defined in claim 17 wherein

said first switch device is a MOS transistor of a first conductivity type;

said second to fourth switch devices being MOS transistors of a second conductivity type.

19. A clock control circuit comprising:

an interpolator receiving a frequency divided signal produced by a frequency dividing circuit receiving a clock signal and a signal obtained by shifting the frequency divided signal in a preset number of periods of the clock to produce a signal obtained on division of a timing difference of said two input signals at a preset ratio of internal division; and

a control circuit for varying value of the ratio of the internal division of the timing difference in said interpolator based on said clock signals.

20. A clock control circuit comprising:

a plurality of (N) interpolators for outputting signals obtained on dividing a timing difference of two input signals with respective different values of a preset ratio of internal division; wherein

of first to nth clocks with respective different phases, two clocks, that is the Ith and the (I+1)st clocks, where I is an integer from 1 to N, with N+1 being 1, are input to the Ith interpolator.

21. The clock control circuit as defined in claim 8 wherein

said interpolator comprises a logic circuit fed with first and second input signals to output results of preset logical processing of said first and second input signals;

a first switching device connected across a first power source and an internal node, said first switching device being fed at a control terminal thereof with an output signal of said logic circuit and being turned on when said first and second input signals are both of a first value;

a buffer circuit having an input terminal connected to said internal node and having an output logical value changed on inversion of the relative magnitudes of the terminal voltage of the capacitance of said internal node and a threshold value;

a plurality of serial circuits connected across said internal node and a second power source in parallel, each of said serial circuits being made

up of a second switching device turned on when said first input signal is of a second value, said third switch device turned on or off based on a control signal from said control circuit, and a first constant current source; and

a plurality of serial circuits connected across said internal node and a second power source in parallel, each of said serial circuits being made up of a fourth switching device turned on in common when said first input signal is of a second value, said fifth switching device turned on or off based on a control signal from said control circuit, and a constant current source.

22. The clock control circuit as defined in claim 8 wherein said interpolator comprises:

a logic circuit receiving first and second input signals to output a result of preset logical processing of said first and second input signals;

a first switching device connected across a first power source and an internal node, said first switching device being fed at a control terminal thereof with an output signal of said logic circuit and being turned on when said first and second input signals are both of a first value;

a buffer circuit having an input end connected to said internal node and having an output logical value changed on inversion of the relative magnitudes of the terminal voltage of the capacitance of said internal node and a threshold value;

a plurality of serial circuits connected across said internal node and a second power source in parallel, each of said serial circuits being made

up of a second switching device turned on when said first input signal is of a second value, said third switch device turned on or off based on a control signal from said control circuit, and a first constant current source;

a plurality of serial circuits connected across said internal node and a second power source in parallel, each of said serial circuits being made up of a fourth switching device turned on in common when said first input signal is of a second value, said fifth switching device turned on or off based on a control signal from said control circuit, and a constant current source; and

a plurality of serial circuits connected across said internal node and the second power source in parallel, each said serial circuit being made up of a sixth switching device and a capacitor;

wherein capacitance value attached to said internal node is determined by a period control signal supplied to a control terminal of said sixth switching device.

23. The clock control circuit as defined in claim 21 wherein

a plurality of (N) of each of said second, third, fourth and fifth switching devices are provided;

K of said third switching devices are turned on by a control signal supplied to a group of said third switching devices, where K is 0 to N;

(N-K) of said fifth switching devices are turned on by a control signal supplied to said group of said fifth switching devices;

signals corresponding to the timings obtained on K-based internal division of the timing difference of said first and second input signals,

in terms of a nth fraction of said timing difference as a unit, are output, with the value of said K being changed to vary the ratio of the internal division of said timing difference.

24. The clock control circuit as defined in claim 23 wherein

the control signal supplied from said control circuit to a control terminal of said third switching device is complemented by an inverter and supplied as a control signal to a control terminal of said fifth switching device corresponding to said third switching device.

25. The clock control circuit as defined in claim 21 wherein

said first switching device is a MOS transistor of a first conductivity type; and wherein

said second to fifth switching devices are MOS transistors of a second conductivity type.

26. The clock control circuit as defined in claim 22 wherein

said first switching device is a MOS transistor of a first conductivity type; and wherein

said second to sixth switching devices are MOS transistors of a second conductivity type.

27. The clock control circuit as defined in claim 22 wherein

said period control signal is supplied from said period detection circuit for detecting a period of the input clock.

28. A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock period of said reference

clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock.

29. The clock control method as defined in claim 28 wherein the output clock of a frequency corresponding to a non-integer frequency with respect to the frequency of said reference clock can be output.

30. A clock control method comprising the steps of:

frequency dividing an input clock by a frequency divider receiving the input clock;

generating a control signal, based on the frequency divided clock, for adding or subtracting by a preset unit value of a phase differential to or from a phase difference relative to the frequency divided clock; and

generating an output clock of the phase difference as set by said control signal.

31. The clock control method as defined in claim 28 wherein

the unit phase difference is variably set by a control signal.

32. A clock control method comprising:

generating first to Nth clocks of respective different phases (termed multi-phase clocks) from an input clock to provide the generated clocks to a selector and wherein

said selector sequentially selects and outputs said first to Nth clocks.

33. The clock control method as defined in claim 28 wherein

the output clock is phase-adjusted by an interpolator outputting a signal, a propagation delay of said signal corresponding to division of

timing difference of two clock signals to vary ratio of internal division of timing difference of said interpolator to enable outputting of an output clock of a frequency which is an non-integer frequency of the input clock frequency.

34. A clock control circuit comprising:

a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by adding to the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said reference clock while said n is an positive integer, and whereby a frequency of the output clock is $1/(tCK+\Delta\Phi)$.

35. A clock control circuit comprising:

a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by subtracting from the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said reference clock while said n is an positive integer, and whereby a

frequency of the output clock is $1/(tCK-\Delta\Phi)$.

36. A clock control circuit comprising:

a control circuit unit comprising: an adding circuit that increments an output on receipt of an input clock pulse by a predetermined unit m, wherein the m is a positive integer and is variably set; and

a decoder that decodes the output of the adding circuit to generate a control signal;

and a phase adjustment circuit that receives the input signal and the control signal to generate an output clock wherein a phase of said output clock to a corresponding edge of the input clock is incremented by a unit phase differential value $m\Delta\Phi$, on each cycle of said input clock, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said input clock, said n being an positive integer, whereby a frequency of said output clock is $1/(tCK+m\Delta\Phi)$.

37. A clock control circuit comprising as define in claim 36 comprising

a circuit that receives the input clock and generates first and second signals from the input clock, between edges of said first and second signals a preset timing difference being provided,

wherein said phase adjustment circuit comprises an interpolator that receives said first and second signals and generates the output signal having a propagation delay corresponding to a time of an internal division ratio of the timing difference between said first and second signals, said internal division ratio being changed by said control signal on each cycle of one of said first or second signal.